SYSTEM AND METHOD FOR USING A LEARNING SEQUENCE TO ESTABLISH COMMUNICATIONS ON A HIGH-SPEED NONSYNCHRONOUS INTERFACE IN THE ABSENCE OF CLOCK FORWARDING

ABSTRACT OF THE DISCLOSURE

A memory system includes a memory hub controller that sends write data to a plurality of memory modules through a downstream data bus and receives read data from the memory modules through an upstream data bus. The memory hub controller includes a receiver coupled to the upstream data bus and a transmitter coupled to the downstream data bus. Similarly, each of the memory modules includes a receiver coupled to the downstream data bus and a transmitter coupled to the upstream data bus. Each receiver includes a receive clock generator that is synchronized by coupling a known pattern of data to the receiver. The receiver determines which phase of the receive clock best captures the known pattern and uses that receive clock phase during normal operation.